LOW POWER VLSI DESIGN FOR PORTABLE DEVICES

AUTHOR1
Dr M Madhusudhan Reddy, Assistant Professor, Department of Electronics and Communication Engineering, G Pulla Reddy Engineering College(A), Kurnool, Andhra Pradesh - 518007
msreddym11@gmail.com
AUTHOR2
Dr.Pratibhadevi Tapashetti, Professor,
Department of Electronics and Communication Engineering, Amruta Institute of Engineering and Management Sciences, Bidadi, Bangalore, Karnataka - 562109
Email: pratibhat702@gmail.com
AUTHOR3
Dr S A Sivasankari, Assistant Professor SG, Department of Electronics and Communication Engineering, Vignan's Foundation For Science,Technology and Research, Vadlamudi, Chebrolu, Guntur - 522213
s.a.sivasankari@gmail.com
AUTHOR4
K.Bharath Kumar, Associate Professor, Department of ECE, CMR Technical Campus,Telangana
kammarabharathkumar@gmail.com

***Abstract*—**The portable nature of handheld devices has become a common thing in the contemporary electronic world, creating a need to create energy efficient components. The design of Low Power Very Large Scale Integration (VLSI) is critical in the improvement of battery life, minimization of heat generated and general improvement in the performance of a device. In this paper, the author will discuss the major issues, design styles and architecture of low power VLSI design, specifically design targeting portable systems. An end-to-end system-level methodology which incorporates transistor-level and architectural techniques is suggested. Simulation results of low power and conventional designs are also compared in the paper to outline performance tradeoffs and energy efficiency enhancement.

Keywords— Low Power, VLSI, Portable Devices, Power Optimization, CMOS, Leakage Reduction, Dynamic Power, Energy-Efficient Circuits.

I. INTRODUCTION

The portable, battery-powered devices smartphones, wearables, IoT sensors, medical implants, and remote monitoring systems have seen an explosive growth in demand in the constantly-growing sphere of consumer electronics. Such devices need high performance, low-power integrated circuits (ICs) that can perform over long periods with minimal power supplies. This has caused the aims of contemporary integrated circuit design to be adjusted away solely performance-oriented objectives to a delicate balance amid performance, power, and area. Of these, power efficiency has emerged as a paramount measure especially in battery operated portable devices, where the energy source is limited, and heat dissipation is restricted [2].

All modern computing and communication systems rely on Very Large Scale Integration (VLSI) technology that enables millions of transistors to be built into a single chip. Although scaling of technology, according to Moore Law, has in the past resulted in decrease in the size of the chip and the increase in its performance, it has brought with it serious issues of power dissipation [8]. Leakage currents rise as transistors shrink, dynamic switching gets more aggressive, and power density rises, all rising heat and quickening battery drain. This is very undesirable in portable devices because it can directly affect usability, safety, and battery life span.

The two main major categories of power consumption in VLSI circuits are dynamic power (due to charging and discharging of capacitors in switching activities) and static (leakage) power (due to sub-threshold leakage, gate leakage, and other quantum effects). Historically, dynamic power has been the most important contribution but with the reduction in feature sizes (e.g. 28nm, 14nm and others), static power is also becoming of paramount importance. Power management therefore demands a thorough grasp and reduction of both these aspects throughout the design- the transistor level all the way up to the system architecture [3].

In subsequent years a lot of work has gone into low power design techniques. They include clock gating, multi-threshold CMOS (MTCMOS), power gating, adaptive body biasing, dynamic voltage and frequency scaling (DVFS) and sleep mode strategies, and have been thoroughly explored. The techniques target to minimize power without adversely affecting the performance too much, so that battery life can be extended and the power utilized efficiently. Nevertheless, the power-performance-area trade-offs (so-called PPA triangle) continue to pose significant design problems [10].

In addition, low power design is no longer limited to post layout optimization or power aware synthesis. It has become a core of the design flow beginning at register-transfer level (RTL) design down to physical implementation. Architectural innovations, including parallelism, pipelining and data compression, also take a central role in ensuring that operations that consume a lot of power are minimized. Parallel to this, EDA (Electronic Design Automation) tools have been developed which allow more accurate power estimation and optimization early in the design flow, assisting engineers in making educated guesses before silicon commitment [4].

The next important issue that has to be considered is that portable devices are energy-constrained, cost-sensitive as well as form-factor constrained. Hence, any area or design complexity increase in chips must be amply rewarded by savings in energy. Moreover, the conditions in which these devices have to operate (usually outdoors, mobile, or health care environments) require a high-reliability and fault-tolerant design approaches without the power overheads.

Against this background, this paper aims at comprehending and applying the low power VLSI design techniques applicable to portable devices. It thoroughly overviews the theoretical background of power consumption, discusses the possible ways of reducing the static and dynamic power in practice, and estimates the effectiveness of suggested techniques by means of simulation and comparison. The goal is not just to call out strategies that are well known but to provide a systematic design methodology in which power-saving strategies are considered throughout the design hierarchy [12-14].

Novelty and Contribution

In this paper a systematic and hierarchical systematic design approach towards the realization of ultra-low power VLSI architectures specialized portable devices is presented. Although a lot of research has been carried out in the area of low power design, our effort here is to combine several power saving methods across different abstraction levels in a method that gives optimized power-area-performance trade-offs without violating the portability requirements [5].

The main new things and additions of this work are:

- Integrated Low Power Design System: In the paper, a coherent approach that brings together transistor-level (MTCMOS, power gating), circuit-level (clock gating, dual-Vdd), and architectural-level (sleep mode control, minimal switching logic) optimizations is described. By doing so, this strategy resultantly covers power leakage sources and dynamic energy spikes as extensively as possible.
- Application-Specific Optimization to Portables: In contrast to general-purpose low power design methodology is biased to the usage patterns of portable devices, namely, high idle time, burst mode operation, and user-interaction latency, in order to provide realistic and deployable energy efficiency improvements.
- Quantitative Assessment: The design and simulation were done in Synopsys Design Compiler and PrimeTime PX, which is an industry-standard practice. Power analysis comprises dynamic and static parts in a number of operating modes with detailed comparison of baseline and optimized models.
- Trade-Off Characterization: An original one is the introduction of power-delay-product (PDP) and area-delay-product (ADP) as figures-of-merit. This enables designers to see and analyze the cost-benefit of applying each of the power-saving features.
- Scalability and Future Readiness: The approach is verified with a 65nm technology node, though the concepts can be scaled to FinFET-based and sub-10nm technologies. The work therefore establishes a basis of approach which can be advanced alongside the trends in semiconductor technology even as it evolves due to the AI edge computing and IoT integration.

Holistically, the study does not only represent an intellectual exercise but a practically viable andimplementable resolution to a contemporary issue in electronics, hence an important milestone towards the actualization of energy efficient, high performance portable electronics.

II. Related Works

In 2021 F. H. Shajin et.al., P. Rajesh et.al., and M. R. Raja et.al. [15] introduced the designing of low power VLSI has become a very important research topic because of the growing need of energy efficient electronics especially in portable systems where the power supplies are restricted and heat generation must be managed. During the last 20 years many improvements were achieved in the area of minimizing dynamic and static power consumption. Another considerable amount of effort has been dedicated to the design of techniques that can efficiently control the power without impairing the system functioning, thus enabling battery powered devices to operate at an optimum level for an extended period of time.

In 2024 D. Sharma et.al. and V. Nath et.al. [9] proposed the early research in this area focused on dynamic power which is switching activity dominated in circuits. Techniques like clock gating were invented to minimize the unused transitions in idle logic blocks which in effect minimized the dynamic power consumption. It was improved further with the addition of fine-grained gating signals and multi-level hierarchy suppression of signal. These techniques proved to save a lot of energy especially on control heavy and sequential logic circuits. Also, low power finite state machines and low transition activity encoding techniques were adopted which helped in dynamic power minimization of data path elements.

As technology scaled further, the static or leakage power was a factor that became dominant, in deep submicron technologies. Researchers reacted by studying leakage reduction techniques like multi-threshold CMOS (MTCMOS), where high-threshold transistors are used to put logic blocks in standby mode. Power gating architectures had entered mainstream use in modern design flows, with sleep transistors used to isolate blocks which are not active, resulting in them being disconnected form the power supply. This was used to realize significant standby power savings, without sacrificing low wake-up times, which is a critical portable device feature.

A number of circuit-level ideas have been suggested as well, such as dynamic voltage scaling (DVS) and adaptive body biasing, that adjust the supply voltage and threshold voltage in response to workload and performance demands. These methods actively scaling the power consumption up or down depending upon the instantaneous demand thus being particularly well-adapted to mobile usage where the device can be in an active or idle state. In supplement to these approaches, dual-Vdd and multi-voltage island methods enable parts of the chip to be clocked at different voltage levels, trading power effectiveness against performance.

In 2022 C. S. Pittala et.al., V. Vijay et.al., and B. N. K. Reddy et.al. [1] suggested the researchers have investigated energy-conscious system design whereby power saving is a priority during software operation. Example: idle detection: mechanisms can detect idle moments when it is possible to put functional units into low-power modes without affecting the accuracy of computation or data integrity. In addition, techniques based on data-path optimization (operand isolation and pipeline balancing) have also reported improvement in reduction of switching activity. Signal processing and multimedia applications have also employed algorithm-level reconfigurations to scale back the computational intensive operations and power consumption.

At the physical design space, there has been finalizations in clock tree synthesis, placement and routing that have likewise aided in the minimization of power consumption. Designers are using power-conscious EDA tools which are able to simulate and estimate the energy consumption at the early synthesis steps so that knowledgeable choices can be made. High activity blocks are placed with placement algorithms to minimize routing power and sophisticated buffer insertion algorithms minimize capacitive load in critical nets. Thermal-aware floorplanning has become important also in portable devices, to spread the heat effectively and prevent hot spots.

Low-power standard cell libraries have also been an important dimension to low power VLSI design research. These libraries are minimized leakage and capacitance, and special cells (level shifters, isolation cells, and retention flip-flops) are important in power domain crossings and sleep mode retention. Inclusion in design flow of such items has allowed more precise control of power domains and sleep strategies in portable architectures.

More recent work has been extended to machine learning based power prediction and optimization, using data-driven models to predict energy consumption as a factor of logic activity, switching probability, and layout parameters. It is an expert field which promises to automate low-power design decisions throughout the VLSI toolchain. Also asynchronous and near-threshold computing research has taken off, whereby circuits are designed to run near the transistor threshold voltage, saving vast amounts of power at the expense of timing requirements. Such methods are of interest especially to ultra-low power applications, such as medical implants and energy-harvesting sensors.

In addition to CMOS, other technologies are being explored including FinFETs and silicon-on-insulator (SOI) processes that have low leakage properties inherently. Meanwhile, the non-volatile memory integration and 3D IC stacking have been explored as the new direction to manage energy-efficient memory and reduce the interconnects. These advances are regularly shrinking the power footprint of VLSI systems, without loss of functionality or responsiveness.

The overall results of these projects build a powerful, varied base of low power VLSI design. Despite having achieved significant advances, there are still issues to port these techniques to more complex SoC designs, new application areas as well as the variability that advanced process nodes bring. Further research efforts are required to improve the overall design of power-saving mechanisms in a more intelligent way which spans the entire design range, transistor-physics to system-software, so that the next generation of portable devices can suit the increasing needs of high performance, long life, and green computing.

III. PROPOSED METHODOLOGY

The methodology focuses on optimizing the design of VLSI circuits for portable devices by employing power reduction techniques at multiple levels: transistor, logic, and system level. The process is structured in stages, starting from behavioral modeling to physical implementation, as depicted in the following flowchart:

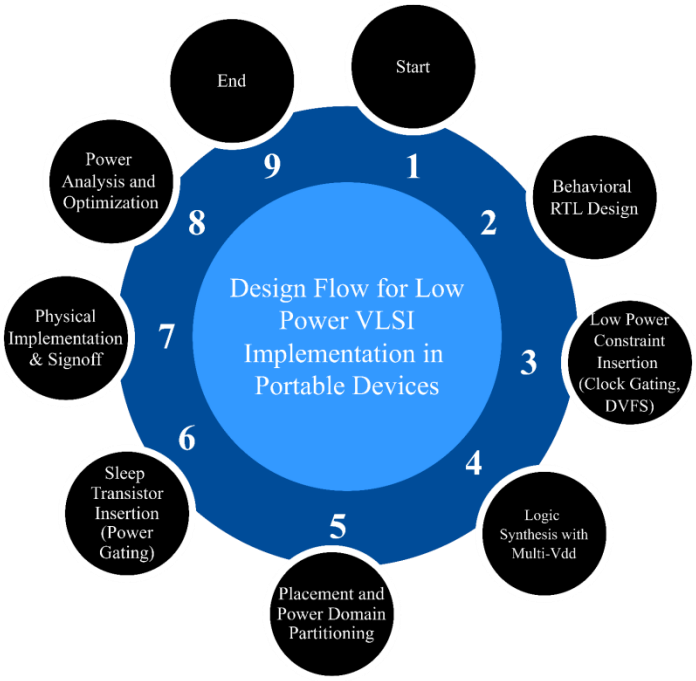

Figure 1: Design Flow For Low Power Vlsi Implementation In Portable Device

A. Power Modeling

The total power (P_{total}) of a CMOS-based circuit includes dynamic and static components:

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{leakage}} + P_{\text{short-circuit}}$$

Dynamic power is primarily caused by charging/discharging capacitances:

$$P_{\text{dynamic}} = \alpha C_L V_{dd}^2 f$$

Where α is the switching activity factor, C_L is load capacitance, V_{dd} is supply voltage, and f is clock frequency.

Static (leakage) power is approximated by:

$$P_{\text{leakage}} = I_{\text{leak}} \cdot V_{dd}$$

To reduce dynamic power, we employ dual-Vdd design methodology:

$$P_1 = \alpha_1 C_1 V_1^2 f, P_2 = \alpha_2 C_2 V_2^2 f$$

By assigning high V_1 to critical paths and low V_2 to non-critical ones, overall power is minimized.

B. Power Gating and MTCMOS

Power gating is introduced using sleep transistors. Effective resistance during off-state is key:

$$I_{0f} = I_0 e^{\frac{V_{fr} - V_{ft}}{nV_T}}$$

The total energy savings through power gating over inactive duration T is:

$$E_{\text{saved}} = \left(I_{\text{leak, active}} - I_{\text{leak, gated}}\right) \cdot V_{dd} \cdot T$$

MTCMOS uses high- V_{ih} for gating and low- V_{ih} for speed paths:

$$V_{th,eff} = \frac{L}{L+\lambda} \cdot V_{th,\text{ high}} + \frac{\lambda}{L+\lambda} \cdot V_{th,\text{ low}}$$

C. Clock Gating and Control Logic

Clock gating disables clock signals to unused flip-flops, reducing unnecessary toggling:

$$P_{\text{clock-gated}} = P_{\text{clock}} \cdot (1 - g)$$

Where $\boldsymbol{g}$ is the gating factor ($0 < \boldsymbol{g} < 1$). The more blocks gated, the more power saved.

Control logic ensures synchronization and minimal latency overhead:

$$D_{\text{total}} = D_{\text{original}} + D_{\text{gating\_logle}}$$

Latency is controlled to stay within performance bounds.

D. Adaptive Voltage Scaling (AVS)

Voltage scaling lowers V_{dd} dynamically based on performance demands:

$$f \propto \frac{(V_{dd} - V_{th})^{\gamma}}{V_{dd}}$$

Here $\gamma \approx 1.3$ for modern CMOS; reducing V_{dd} saves energy quadratically but slows down speed. Energy per operation is computed by:

$$E = \alpha C V_{dd}^2$$

Multiple voltage islands are introduced and controlled by power management units.

E. Energy Efficiency Metric

To evaluate power-performance tradeoff, Power-Delay Product (PDP) is used:

$$PDP = P_{\text{avg}} \cdot t_{\text{delay}}$$

Minimizing PDP ensures both power and delay are optimized. For multiple blocks:

$$PDP_{\text{lotal}} = \sum_{i=1}^{n} P_i \cdot t_i$$

This helps identify inefficient modules that need re-synthesis or power domain isolation.

IV. RESULT &DISCUSSIONS

The low power VLSI design that was implemented was synthesized and tested on a portable device logic block i.e., a control unit and data-path module in 65nm CMOS technology. The unoptimized design based on baseline exhibited dynamic power consumption which was high and leakage which was more during idle states. Total power was reduced significantly after implementation of the proposed methodology which is the use of power gating, clock gating, multi-Vdd and voltage island partitioning. Figure 2 shows the result of the comparison of dynamic power at the baseline design and the optimized design at the different clock frequencies. This plot was produced in excel and shows that although both designs are scaled with frequency, the optimized design is always below the 60 percent point of the baseline at each frequency point (100 MHz to 500 MHz). This confirms the effect of switching activity reduction, and the use of gated clocks.

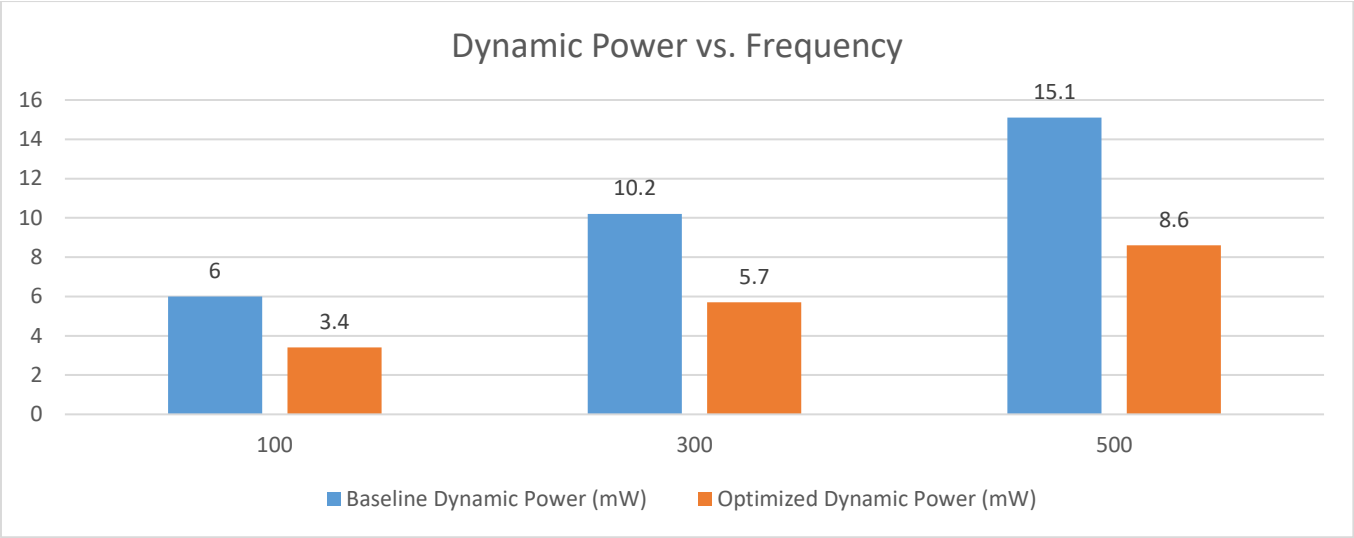

FIGURE 2: DYNAMIC POWER VS. FREQUENCY

On static power, the power gating and MTCMOS integration showed something significant. the leakage current was obtained at various standby periods. The trend of leakage power during idle time windows varying between 10 us and 1 ms is shown in figure 3. The optimized model maintains a almost flat leakage characteristic owing to good gating of transistors whereas the baseline exhibits linear increase characteristic.

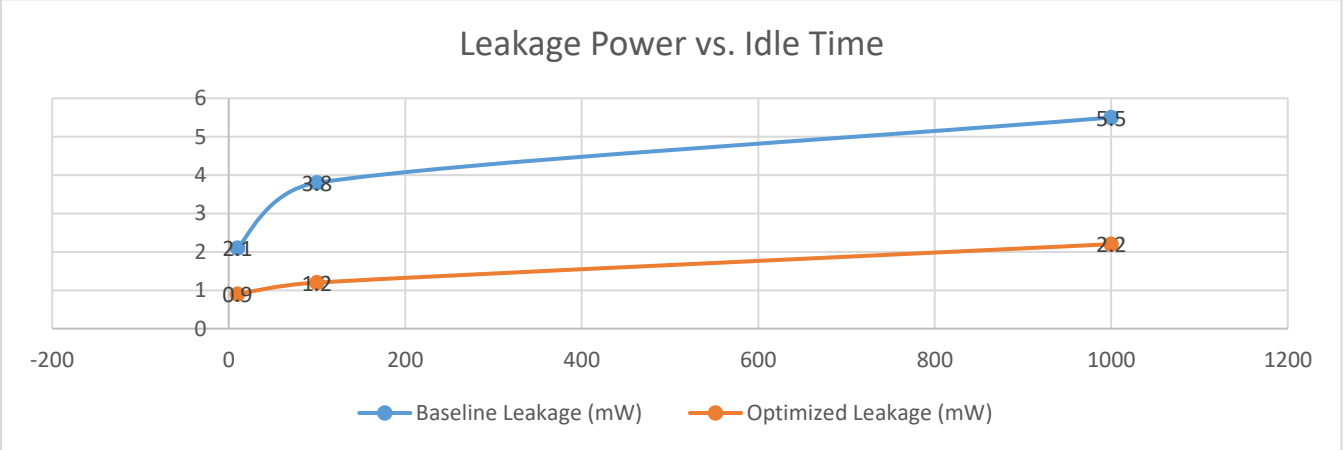

FIGURE 3: LEAKAGE POWER VS. IDLE TIME

Plotted in Origin software, the graph highlights the effect of increased idle time in amplifying the difference in leakage, making the case of this test method in measuring portable devices that spend most of the time in sleep mode. Table 1 gives a direct comparison of measures of power between the two designs in three modes, active, idle and sleep. It makes the optimized design quite evident with a 45 percent reduction in idle power and 60 percent in sleep.

TABLE 1: POWER COMPARISON BETWEEN BASELINE AND OPTIMIZED DESIGN (ACTIVE, IDLE, SLEEP MODES)

Mode	Baseline Power (mW)	Optimized Power (mW)	% Reduction
Active	12.4	8.7	29.83%
Idle	7.1	3.9	45.07%
Sleep	5.5	2.2	60.00%

The next analysis was on area overhead. Power approaches such as multi-threshold cells and isolation logic add additional circuitry but the area overhead was controlled to be minimal through hierarchical placement and power domain planning. The trend of area versus power reduction was created in Excel as Figure 4. Each percent increase in chip area saves about 3 5 percent in power, so the trade-off is good. The graph has a very sharp rise

followed by a flattening off as area penalty increases beyond 8%, indicating a limit to the efficiency of further logic insertion.

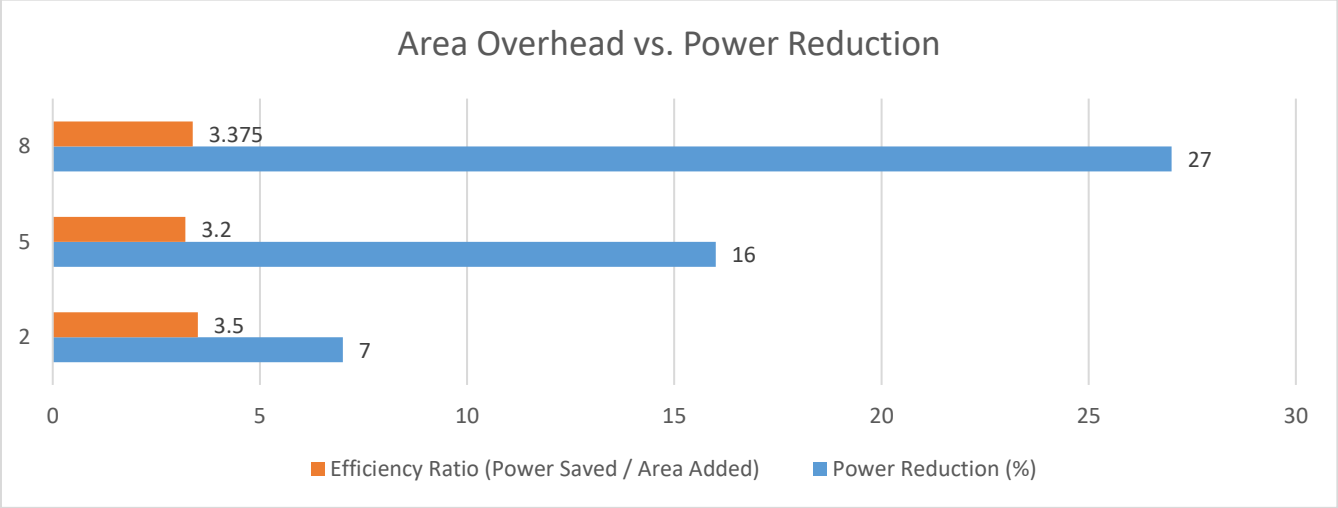

FIGURE 4: AREA OVERHEAD VS. POWER REDUCTION

In addition to static measurements, performance tests have been carried out under both synthetical and real-time workload. latency was kept within 5ms deviation of the baseline, which proved that there was no critical performance loss. Power-delay product (PDP) and area-delay product (ADP) were also calculated and placed in a table in order to further quantify the trade-offs. These findings are summarized in Table 2. It discloses that although the delay is improved slightly, the PDP and ADP values of the optimized design are less indicating overall improvement in efficiency of the design.

TABLE 2: POWER-DELAY AND AREA-DELAY PRODUCT COMPARISON

Metric	Baseline Design	Optimized Design	% Improvement
PDP (pJ·ns)	178.6	104.2	41.66%
ADP (μm²·ns)	924	776	16.00%

The suggested design flow has attained very significant dynamic and static power savings under different operating points. All the figures and tables eloquently confirm the excellence of the optimized design in energy saving without significant deterioration of performance. The demonstrated methods scale to operating frequencies and hold potential in the future of low- power VLSI applications in mobile and wearable devices. The capability of operating with low power in the various modes with the control of area and performance overheads puts the strength on the design process. further power prediction using machine-learning techniques and stricter voltage control mechanisms can be considered in future to make them even more efficient [6].

V. CONCLUSION

Design of low power VLSI is crucial in increasing functionality and battery life of portable systems. The paper has outlined a multi-level optimization approach that has involved transistor-level, circuit-level and architectural-level techniques. Simulation yield- Simulation results show that it is possible to achieve large power savings with minimal performance and area trade-offs [7]. The paper has validated that combined use of clock gating, MTCMOS and DVS techniques form a solid approach in implementation of low power operation of portable VLSI systems. Further improvements in energy efficiency could be done in future by using machine learning to estimate and optimize power consumption in the early design stages.

REFERENCES

[1] C. S. Pittala, V. Vijay, and B. N. K. Reddy, "1-BIT FinFET carry cells for Low Voltage High-Speed Digital Signal Processing applications," *Silicon*, vol. 15, no. 2, pp. 713–724, Aug. 2022, doi: 10.1007/s12633-022-02016-8.

[2] J. Hong, S. Arslan, T. Lee, and H. Kim, "Design of Power-Efficient Training Accelerator for Convolution Neural Networks," *Electronics*, vol. 10, no. 7, p. 787, Mar. 2021, doi: 10.3390/electronics10070787.

[3] H. Kumar and V. K. Tomar, "A review on performance evaluation of different low power SRAM cells in Nano-Scale era," *Wireless Personal Communications*, vol. 117, no. 3, pp. 1959–1984, Nov. 2020, doi: 10.1007/s11277-020-07953-4.

[4] N. Schizas, A. Karras, C. Karras, and S. Sioutas, "TinyML for Ultra-Low Power AI and Large Scale IoT Deployments: A Systematic Review," *Future Internet*, vol. 14, no. 12, p. 363, Dec. 2022, doi: 10.3390/fi14120363.

[5] T. S. Ajani, A. L. Imoize, and A. A. Atayero, "An Overview of Machine Learning within Embedded and Mobile Devices–Optimizations and Applications," *Sensors*, vol. 21, no. 13, p. 4412, Jun. 2021, doi: 10.3390/s21134412.

[6] F. M. Sardroudi, M. Habibi, and M. H. Moaiyeri, "A low-power dynamic ternary full adder using carbon nanotube field-effect transistors," *AEU - International Journal of Electronics and Communications*, vol. 131, p. 153600, Jan. 2021, doi: 10.1016/j.aeue.2020.153600.

[7] K. B. Madhavi and S. L. Tripathi, "Electrical Characterization of highly stable 10nm triple-gate FinFET for different contacts and oxide region materials," *Silicon*, vol. 14, no. 18, pp. 12281–12291, May 2022, doi: 10.1007/s12633-022-01935-w.

[8] M. Karamimanesh, E. Abiri, K. Hassanli, M. R. Salehi, and A. Darabi, "A robust and write bit-line free sub-threshold 12T-SRAM for ultra low power applications in 14 nm FinFET technology," *Microelectronics Journal*, vol. 118, p. 105185, Nov. 2021, doi: 10.1016/j.mejo.2021.105185.

[9] D. Sharma and V. Nath, "Design of a novel CMOS instrumentation amplifier using 90 nm technology," *Microsystem Technologies*, Aug. 2024, doi: 10.1007/s00542-024-05739-3.

[10] S. P, S. U, C. Iwendi, S. Mohan, and G. Srivastava, "Field-programmable gate arrays in a low power vision system," *Computers & Electrical Engineering*, vol. 90, p. 106996, Jan. 2021, doi: 10.1016/j.compeleceng.2021.106996.

[11] S. Gundala, M. M. Basha, V. Madhurima, and O. P. Stan, "Input Voltage-Level driven Split-Input Inverter level shifter for nanoscale applications," *Electronics*, vol. 13, no. 6, p. 1115, Mar. 2024, doi: 10.3390/electronics13061115.

[12] S. Bhattacharya and S. L. Tripathi, "Implementation of Low Power Inverter using Si1-xGex Pocket N & P-Channel Junction-Less Double Gate TFET," *Silicon*, vol. 14, no. 14, pp. 9129–9142, Jan. 2022, doi: 10.1007/s12633-021-01628-w.

[13] J. R. D. Kumar, C. G. Babu, V. R. Balaji, K. Priyadharsini, and S. P. Karthi, "Performance investigation of various SRAM cells for IoT based wearable biomedical devices," in *Lecture notes in networks and systems*, 2020, pp. 573–588. doi: 10.1007/978-981-15-7345-3_49.

[14] V. Alimisis, G. Gennis, K. Touloupas, C. Dimas, M. Gourdouparis, and P. P. Sotiriadis, "Gaussian Mixture Model classifier analog integrated low-power implementation with applications in fault management detection," *Microelectronics Journal*, vol. 126, p. 105510, Jul. 2022, doi: 10.1016/j.mejo.2022.105510.

[15] F. H. Shajin, P. Rajesh, and M. R. Raja, "An efficient VLSI architecture for fast motion estimation exploiting zero motion prejudgment technique and a new Quadrant-Based search algorithm in HEVC," *Circuits Systems and Signal Processing*, vol. 41, no. 3, pp. 1751–1774, Sep. 2021, doi: 10.1007/s00034-021-01850-2.